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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,217	08/22/2001	Brent Keeth	DB000575-012	3379

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/29/2002

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,217	KEETH ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *223-237,247-250 and 466-510* is/are pending in the application.

4a) Of the above claim(s) *466-495* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *223-237,247-250 and 496-510* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 223 is rejected under 35 U.S.C. 102(b) as being anticipated by Park (USP 5448199).

Park discloses in figure 3 a voltage reference circuit responsive to an external voltage (ext. Vcc) for supplying a reference voltage (int. Vcc) , comprising: an active reference circuit (10, 20, 30) for receiving the external voltage and for producing a reference signal (at node N2) having a desired relationship with the external voltage; and a unity gain amplifier (50) responsive to the reference signal for producing the reference voltage.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 224, 496 and 497 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (USP 5448199) in view of Shibayama et al. (USP 5554953).

Park's figure 3 shows the active reference circuit comprises a current source (56). Park's figure 3 fails to shows a diode stack having an adjustable impedance. However, Shibayama et

al.'s figure 2 shows a method of replacing diode Qp16 of figure 1 with a diode stack (Qp16 of figure 2) having adjustable impedance for the purpose of capable adjusting the output reference voltage. Thus, it would have been obvious to one having ordinary skill in the art to replace Park's diode 58 (or 57 or both of diode 57 and 58) with Shibayama et al.'s diode stack for the purpose of capable of adjusting the output voltage of the reference circuit.

5. Claims 225-227 and 498-500 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (USP 5448199) in view of Shibayama et al. (USP 5554953) and Furumochi (USP 5473277).

As to claims 225 and 498, Park's figure 3 and Shibayama et al.'s figure 2 shows the diode stack includes a plurality of transistors (Qp31-35) connected in series, with each transistor's gate connected to a common potential (ground), and a plurality of fuses (F0-F4) each for shunting one of the transistors. Shibayama fails to shows each of the plurality of switches selectively shunts of the transistors. However, Furumochi's figures 1-6 show a method of using switches for shunting diodes for the purpose of reversibly controlling the output voltage. Therefore, it would have been obvious to one having ordinary skill in the art to replace Shibayama's fuses with switches for the purpose of reversibly controlling the output voltage.

As to claims 226 and 499, Furumochi's figures 3 and 5 teaches the switch can be controlled by fuse. Therefore, it would have been obvious to one having ordinary skill in the art to use fuses to control the switches because it is seen as an obvious design experiment dependent upon particular environment of use to ensure optimum performance.

As to claims 227 and 500, Furumochi's figure 5 shows a witch (SWO(TN4)) is made of Field Effect Transistor. Therefore, it would have been obvious to one having ordinary skill in

the art to use Field Effect Transistors for the plurality of switches because it is a design choice. Shibayma's figure 2 further shows the plurality of transistors includes a first plurality of field effect transistors.

6. Claims 228-231 and 501-504 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (USP 5448199).

As to claims 228 and 501, Park's figure 3 fails to shows a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a predetermined value. However, because circuit 50 is a unity gain amplifier, the circuit will function the same for circuit 100 connected at the output instead at the input of the amplifier. Therefore, it would have been obvious to one having ordinary skill in the art to connect circuit 100, wherein circuit 100 is the "pullup stage", to the output instead of the input of the unity gain amplifier (50) because is is a design choice.

As to claims 229 and 502, Park's figure 3 shows the pullup stage includes a plurality of diodes (61-63) connected between the external voltage and the reference voltage.

As to claims 230 and 503, from the rejection above, it is inherent that the reference voltage is the external voltage less a voltage drop across the plurality of diodes.

As to claims 231 and 504, Park fails to teach a power amplifier stage for amplifying the reference voltage by a factor greater than unity to provide an output voltage. However, it is well known in the art that amplifier having the gain greater than unity is for providing an output having level greater than the level of input signal. Therefore, it would have been obvious to one having ordinary skill in the art to add a power amplifier having gain greater than unity to the

output of Park's figure 3 for the purpose of providing an output signal greater than the int. Vcc level.

7. Claims 232-237, 247 and 505-510 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayakawa (USP 5184031) in view of Park (USP 5448199).

As to claims 232 and 505, Hayakawa shows in figure 1 a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value and supplying a step down voltage when the external voltage is above the predetermined value. Thus, Hayakawa shows all limitations of the claim except for the detail of the internal stepdown circuit (13). However, Park's figure 3 shows a detail of an internal step down circuit (see the rejection of claim 231). Park's figure 3 having an advantage of providing a stable internal signal. Therefore, it would have been obvious to one having ordinary skill in the art to use Park's internal circuit for Hayakawa et al's internal stepdown circuit (13) for the purpose of providing a stable internal signal.

As to claims 233 and 506, Hayakawa et al.'s figure 2 shows the circuit for supplying includes a switch (14) for shorting a bus carrying the external voltage with a bus carrying the output voltage.

As to claims 234 and 507, Park's figure 3 shows a pullup stage (100) for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a second predetermined value (see the rejection of claim 228).

As to claims 235 and 508, Park's figure 3 shows the pullup stage includes a plurality of diodes (61-63) connected between the external voltage and the reference voltage.

As to claims 236 and 509, from the rejection above, it is inherent that the reference voltage is the external voltage less a voltage drop across the plurality of diodes.

As to claims 237 and 510, from the rejection above it is inherent that the combination supplies an output voltage which increases at a first slope substantially the same as a slope of the external voltage during a powerup range, increases at a second slope substantially less than a slope of the external voltage during an operating range, and increases at a third slope greater than a slope of the external voltage during a burn-in range of the external voltage.

Claim 247 recites similar limitations of claims 232-237. therefore, it is rejected for the same reasons.

8. Claims 248-250 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayakawa (USP 5184031) in view of Park (USP 5448199) and Shibayama et al. (USP 5554953).

As to claim 248, The combination of Hayakawa and Park teaches all limitations of the claim except for the step of draining the current from the circuit node through an adjustable impedance. However, Shibayyama et al. teach in figure 2 a method of using diode stack (Qp16) having adjustable impedance for adjusting output voltage level. Therefore, it would have been obvious to one having ordinary skill in the art to replace Park diode 58 (or 57 or (58 and 58)) with Shibayama et al.'s diode stack for the purpose of capable of adjusting the output level of the reference circuit (see the rejection of claim 224).

As to claim 249, from the rejection above, it is inherent for the step of adjusting the impedance to modify the reference signal.

As to claim 250, it is inherent for the step of adjusting the impedance includes the step of opening a fuse.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
May 22, 2002

Terry D. Cunningham
Primary Examiner